

## Abstract

A method and apparatus for resuming operations from a low latency wake-up low  
5 power state. One embodiment provides a system including a processor, an operating  
system, and a memory subsystem that requires initialization commands to exit a memory  
low power state. Control logic detects exit from an operating system low latency low  
power state and responsively generates a plurality of initialization commands to remove  
the memory subsystem from the memory low power state prior to deasserting a stop  
10 clock signal and allowing execution to resume.